Optimization of Ternary Combinational System

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Abstract— This paper presents basic concept about ternary number system, this paper gives us idea about symbol and truth table of ternary gates it also gives novel method for defining, analyzing and implementing the basic combinational circuitry with minimum number of ternary gates. This paper provides concept of Boolean algebra to ternary number system. The 3:1Multiplexeris designed using ternary gates to realize combinational circuitry that provides complete, concise, implementation-free description of the ternary functions involved. Half and full adder circuit implemented using ternary gates the method is useful in analyzing the complex ternary functions and reduction of gate count. This paper also presents a survey on ternary switching algebra.

Index Terms— Gate count; Multi-valued logic; Ternary Switching Levels, Kernaugh Map, Ternary gate, VLSI,

1 INTRODUCTION

The fundament of today's digital technology age is binary logic. The time when Shannon expressed the behavior of electrical switches in Boolean algebra, he overlay the ramp to an industrial development which is recognized as beginning of one of the most revolutionary economic changes ever. Binary logic technology has come across the dramatic changes and advances. Earlier from electro-mechanical to electronic switches by using electronic tubes (1919) like triode, pentodes, then from tubes to transistors (1948) and from transistors to LSI (1958) and VLSI (1970)circuits. Although efficient and powerful, binary logic is not the most efficient and powerful switching logic. Non-binary logic or Multiple Valued Logic (radix>2) has been around for quite a while and is known as Multi-Valued Logic or Many Valued Logic. In this paper it will be referred to as MVL hereafter. The subject of MVL is also known as Multi-Valued, Multiple-Valued or Many-Valued logic. In case of 3-Valued logic (radix = 3) the term 'Ternary' logic is used & term 'Quaternary' logic (radix = 4) for 4-Valued logic and so on up to 'n' values. Multi-Value logic is regarded as a switch with more than two states [1].

Such as a three- value switch with logic states '0', '1' and '2', 4-value switch with logic states '0', '1', '2' and '3' and so on up to 'n' values.

MVL has been the topic of most interest of many researchers over the last 50 years. From 1971 there has been an annual symposium devoted exclusively to the object. Moreover, a large number of technical papers have published together with numerous survey articles. Much of the ancient work is purely theoretical nature concerned with the completeness of the function with sets of operator, function minimization and similar problems from the switching theory and logic design. Work on hardware implementation of multiple value devices has been more recent. The use of Multi-Valued logic ranges from various applications to VLSI technology and design techniques [2].

There are three directions for the work in MVL. Due to pressure to reduce interconnection complexity and reduce chip area on VLSI, it is giving motivation for the investigation of many different hardware implementations of MVL systems. The largest commercial use of Multiple-Valued logic is in the area of MVL memories. The MVL can be used to overcome existing difficulties in the analysis of problems in binary digital systems, such as the design of fault simulators. Finally there is still ongoing work in the general area of switching theory to yield the best methodologies for the implementation of multi-valued systems.There are two modes of operation in MVL. Those are voltage mode operation and current mode operation Figure 1.1 shows operation modes of MVL. In voltage mode operation, logic state is specified in terms of distinct voltage levels i.e.v1, v2….vnand in current mode logic, state is multiple of lowest logic current level state ,i.e.,logic state for current mode is XI1, XI2--XIn Where*x* is reference current:

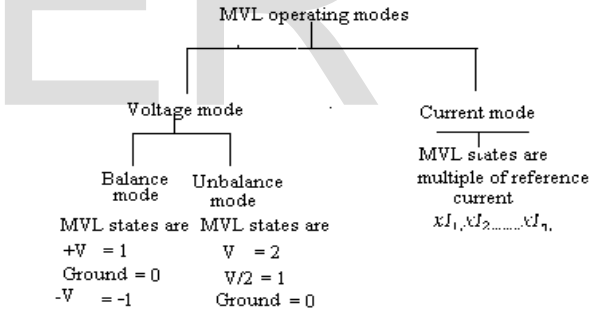


Figure 1.1: MVL operating modes

Where 1,-1, 0 and 2 …n are the logic levels for operation in voltage mode and xI1 xI2…xIn for current mode. The figure 1.2 is a representation for Ternary logic.

Modern technical work have shown advantages of using Multi-Valued logic where the natural question is whether there exists a practical radix other than 2 that would produce circuits with greater saving in components, without loss of speed? Answer to this is 'Yes' and it is Multi Valued Logic.

1.1 Preliminary of Ternary Logic

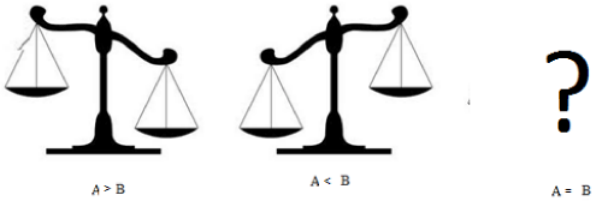
In existing binary digital system, the output of the system is decided by considering two input conditions i.e. either ON (Favorable or true logical level 1) or OFF (unfavorable or false logic at logic level 0) leaving behind the third conditions i.e. when both the input conditions are same, here decision is consider as don't care or it is discarded by the system. Such situation generally occurs in sequential circuit design. Consider a digital system where both the inputs are same, i.e., either 00 or 11as shown in figure 1.2.

Hear in binary system output will be uncertain or will be same as

that of previous state of the system but in practice, system must give the output that will satisfy both the input conditions mentioned previously. It is shown in figure 1.2 here the system gives the output which is balanced and this state is regarded as third state i.e. can't say or can't make any decision. So to make third decision the radix of the system must be greater than 2. Here the third logic level is introduced whose system radix is greater than 2.Alexander [1964] showed that natural base (e ≈ 2.71828) is the most efficient radix for implementation of switching circuits. It seems that most efficient radix for the implementation of digital system is 3 than 2. Ternary logic system, meaning that it has 3 valued switching. Ternary system has several important merits over binary. It can be listed as reductions in the interconnections require to implement logic functions, thereby reducing chip area, more information can be transmitted over a given set of lines, lesser memory requirement for a given data length. Besides this serial & some serial-parallel operations can be carried out at higher speed [1-3]. Its advantages have been confirmed in the application like memories, communications and digital signal processing, and so on [12].

Russian first ternary computer "SETUN" and "SETUN 70" was developed at Moscow state university in 1960.It was found that ternary computer is very favorable for seizing of application simplicity of programming in codes, other than permitted to design a few interpreter. Few of the example of implementation of ternary logic systems are three value counter which greatly simplifies the counter circuitry based on two value logic, Three valued memory based on multi valued logic can considerably reduce the memory size required to store than it requires by using two value logic, the implementation of cyclic convolution where significant advantage can be gained by using ternary digital hardware namely an increased maximum sequence length and can be achieved without increasing the complexity of digital hardware. The current mode CMOS circuits have application in digital signal processing and computing [17].

The three value logic offers particular advantages in digital signal processing applications (Convolution, FFT) etc. For example, an increased maximumsequence of length can be achieved by implementing ternary logic system in DSP.



A) Favorable decision B) Unfavorable decision C) Don't care

Figure 1.2: Binary decision making

A) Favorable decision B) Unfavorable decision C) Can't make any decision

Figure 1.3: Natural decision making

1.2 Ternary Switching Algebra

Let a system be L whose elements called propositions or statements are valued in the set {0, 1, and 2} thatis denoted by Z3. If X is a proposition, the value of X can be seen as a mapping *V: L → {*0, 1, 2} such that:

0 if X is false

V(x) = 1 if X is intermediate

2 if X is true

Ternary has the logic levels '0' corresponding to logic-0 in binary (also called zero element or low voltage), '1' corresponding to an intermediate stage (also called Meta stable state) and '2' corresponds to logic-1 in binary(Also called universal element or high voltage). The intermediate state can be metaphorically thought of as either true or false. The binary logic is limited to only two states '1' and '0', where as MVL is a set of finite or infinite number of values. In a standard CMOS process, the three supply voltages are vdd, vdd/2 and ground.

Ternary logic gates are the basic building blocks in realizing combinational and sequential logic functions. The implementation is based around (bipolar transistors, MOSFETs etc.) a basic switching elements, which isReferred to as T-Gates[8] the Ternary gate called T-gate qualifies as a universal element in several different senses. Firstly, it should be logically complete with simple operation. Secondly, it should be easily implementedwith its straightforward construction. Thirdly, it should possess two essential elements that must be embodied in any logic gate, namely, logic-value thresholding and logic-signal connection of switching [15]. This functional completeness of T-gate is the property of a set of compositions which enables one to synthesize any arbitrary switching function within a particular class. There are several algebras available for the design of ternary switching functionsamong which, the Post and the Modular algebra have the advantages of similarity with ordinary algebra. In system L, a set of operators namely unary and binary are defined.

For x, y, z €L, there exists equivalence (=) operation, such that

x = x

If x = y, then y = x

If x = y and y = z, then x = z

A general ternary inverter (GTI) is a basic unary operator with one input *x* and three outputs. Therefore, the implementation of ternary inverter requires three inverters namely negative ternary inverter (NTI), standard or Simple ternary inverter (STI) and positive ternary inverter (PTI) forming an operator set that is complete in logic sense. This basic ternary inverter is used for constructing ternary AND/NAND, ternary OR/NOR etc. They are represented and tabulated as shown in Table I and Fig.3:

$$STI \equiv X^{I} = 2 - x \quad (1)$$

$$PTI, NTI = \begin{cases} X^{I} & \text{if } X^{I} \neq I \\ 2 - I & \text{if } X = I \end{cases} \quad (2)$$

Where i takes the value of 2 for PTI and 0 for the NTI operator. The minus sign represents arithmetic subtraction

Symbols for PTI STI of NTI are shown in Figure 1.5

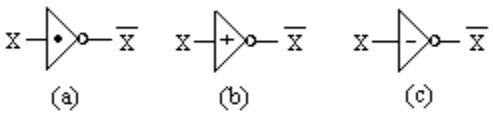


Figure 1.4: Symbols for Inverters (a) STI (b) PTI (c) NTI

Table 1: For ternary inverter

X	x^{o}(NTI)	X^{2}(PTI)	x^{1}(STI)
0	2	2	2
1	0	2	1

2	0	0	0

When n = 1, one-variable functions f(x) exist with 3^{3^1} = 27 modal functions called Literals as shown in Table II. Similarly, there are 3^{3^2}= 19683 two-variable functions and 3^{3^3}=76255974849 three-valued functions Literal is denoted by $a\ X_{i,}^{a}$where a_I= 0,1,2,01,02 and 12 and is defined as given here

X^I=0 if $X \neq I$ (3)
2 if X = I
Where I = 0, 1&2:

$X^{01}=X^0 + X^1$ (4)
$X^{12}=X^1 + X^2$ (5)
$X^{02}=X^0 + X^2$ (6)
$X^{01} \bullet X^{12}=X^1$ (7)
$X^{01} \bullet X^{02}=X^0$ (8)
$X^{02} \bullet X^{12}=X^2$ (9)
$X^0 + X^1 + X^2 = 2$ (10)

Table 2: Function Table of Unary Functions

X	X^o	X^1	X^2	X^{o1}	X^{12}	X^{o2}
0	2	0	0	2	0	2
1	0	2	0	2	2	0
2	0	0	2	0	2	2

It can be proved that the complement or negation of literals (X^1) give the following observed Eq. (12-15) which are helpful in reduction of ternary gates during implementation. The negation is defined and represented as shown in Fig.4 and Eq. (11)

COM (X^i) or NEG(X^i) =x^I = 0 if X=I (11)
2 if X ≠I (12)

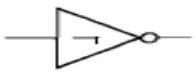


Figure 1.5: Symbol for negation

$\overline{X^2} = X^{01}$ & $\overline{X^{01}}=X^2$ (13)

$\overline{X^1}=X^{02}$& $\overline{X^{02}}=X^1$ (14)

$\overline{X^0}=X^{12}$&$\overline{X^{12}}=X^0$ (15)

$\overline{0}=2$ & $\overline{2}=0$ (16)

This observed result is used to show the reduction in gate count and also in simplification of ternary function.
The operation of addition (+) and multiplication (.) on L, which can be called Ternary OR (TOR) and Ternary AND (TAND) respectively It is represented by following equations and tabulated as shown in **Table 3** and Fig.5 and 6. Logic Sum or TOR:

X1 X2 … Xn=MAX(X1,X2,…,Xn) (17)
Logic Product or TAND:
X1 +X2 +…+Xn =MIN(X1, X2,…,Xn)
Similarly, TNAND is:

$\overline{X1 \bullet X2 \bullet \ldots \bullet Xn} = MIN\ (\overline{X1\bullet}, \overline{X2\bullet \ldots \bullet Xn})$ (18)
TNOR is:

$\overline{X1+ X2+... +Xn} = MAX\ (\overline{X1+ X2+ ...+Xn})$ (19)

Table3: Truth table of ternary basic gate

A	B	TNAND	STNAND	PTNAND	NTNAND	TOR	STNOR	PTNOR	NTNOR
0	0	0	2	2	2	0	2	2	2
0	1	0	2	2	2	1	1	2	0
0	2	0	2	2	2	2	0	0	0
1	0	0	2	2	2	1	1	2	0
1	1	1	1	2	0	1	1	2	0
1	2	1	1	2	0	2	0	0	0
2	0	0	2	2	2	2	0	0	0
2	1	1	1	2	0	2	0	0	0
2	2	2	0	0	0	2	0	0	0

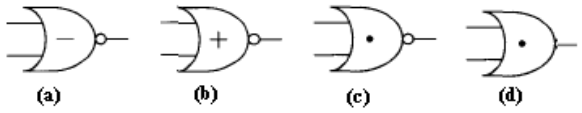


Fig.5: Symols of Max Operator
a) NTNOR (b)PTNOR (c) STNOR & (d) TOR

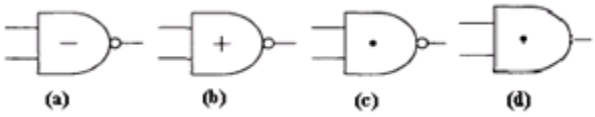


Fig.6: Symbols of MIN operator

(a)NTNAND (b) PTNAND (c) STNAND and (d) AND

Clearly (L, +,) is a distributive lattice with zero element(0) and universal element(2) Thus the following laws hold for any x, y, z € L:

Idempotent: X+X=X
X ●X=X
Commutative: X+Y=Y+X
X ●Y=Y●X
Associative: (X+Y) +Z=X+(Y+Z)
X●(Y ●Z) = (X ●Y) ●Z

Absorption: X+ X ●Y =X
X●(X+Y) = X

Distributive: X+Y●Z= (X+Y) ●(X+Z)
X●(Y+Z) =X●Y+X●Z

It is evident that laws of identity elements, holds here:

X + 0 = X (20)
X • 0 = 0 (21)
X + 2 = 2 (22)
X • 2 = X (23)
X • 1= 1(for cases X ≠0) (24)
X+1 = 1(for cases X ≠2) & 2(for x=2) (25)

DeMorgan's Theorem holds for ternary logic when the three types of inverters are used:

$\overline{(X+Y)}^{o} = \overline{X}^{o} \bullet \overline{Y}^{o}$ (26)

$\overline{(X \bullet Y)}^{o} = \overline{X}^{o} + \overline{Y}^{o}$ (27)

$\overline{(X+Y)}^{1} = \overline{X}^{1} \bullet \overline{Y}^{1}$ (28)

$\overline{(X+Y)}^{2} = \overline{X}^{2} \bullet \overline{Y}^{2}$ (30)

$\overline{(X \bullet Y)}^{2} = \overline{X}^{2} + \overline{Y}^{2}$ (31)

$\overline{\overline{X}}^{1} = X$ (32)

Ternary Ex-OR function is mod-3 addition of ternary numbers. Modulo-3 sum is the sum of two integers ignoring the carry digits in the addition. Modulo-3 addition is an important function, since so many redundant Code techniques use half-adding functions it is denoted and expressed as given in Fig.7 and Table 4

X ex-or Y=MODSUM (X, Y)=(X + Y) mod 3 (33)

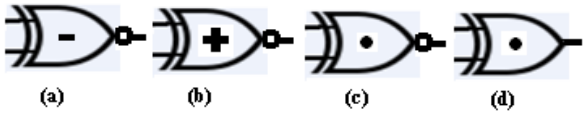


Fig.7: Symbols of MODULO SUM operator

Table4: (a) NTEQV (b) PTEQV (c) STEQV and (d) TXOR

A	B	TXOR	STEQV	PTEQV	NTEQV
0	0	0	2	2	2
0	1	1	1	2	0
0	2	2	0	0	0
1	0	1	1	2	0
1	1	2	0	0	0
1	2	0	2	2	2
2	0	2	0	0	0
2	1	0	2	2	2
2	2	1	1	2	0

Ternary functions of one or more variables may be represented in truth table or K-map form or algebraically in canonical form as a product of sum or sum of product. According to Expansion theorem [14]

any ternary function f(Xl,X2,...,Xn) may be generated from (Xl, X2,...,Xn) by means of (+), (.) and the unary functions X 0 , X 1 , X2 as given here

f(Xl,X2,.., Xn) =2•F2(Xl,X2 ..... Xn)+1•F1(Xi,X2, ...,x n)+0•F0(Xl,X2,... Xn)

That is, f = 2 • F2 + 1 • F1 + 0 • F0 (34)

Where Fk equals 2, when value of the function f equals k, otherwise, it is 0. Applying equations (21) and (23) to the preceding equation, the function may be represented by f = F2+1 • F1 for canonical Sum of Product form and f= F2 • (1+ F1) for canonical Product of Sum form.

2. DESIGN OF TERNARY CIRCUITS

An approach for implementing ternary function is to convert given ternary variable into unary variable using ternary to unary decoder as shown in Fig.1.6. The other circuit design and concepts can also be found in reference:

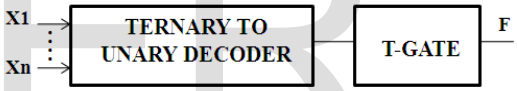
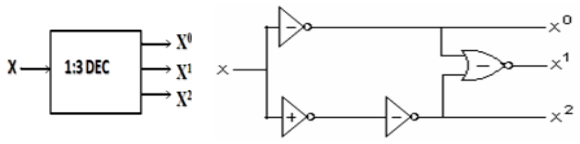


Fig.1.6: Implementation of ternary function

2.1 Design of Decoder and Obtaining Literals

To design ternary circuits, we start with the design of decoder which is a basic building block as shown in Fig.1.7, which operates according to the Table 2:



1.7: Block diagram and Circuit diagram of 1x3 Decoder

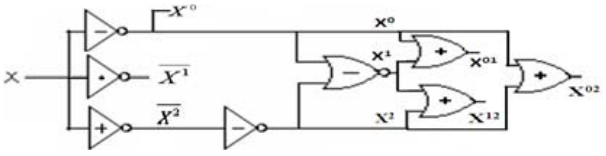


Fig.1.8: Circuit for obtaining Unary functions

A decoder is a combinational circuit that converts the ternary information from n input lines to 3n unique output lines Design to obtain the literals is also shown in Fig.1.8.

2.2 Design of Multiplexer

A ternary multiplexer is a combinational circuit that selects

one of the 3n input lines based, on a set of n selection lines and directs it to a single output line. The design of 3x1 multiplexer (MUX) is as presented in Fig.1.9 and operates as given in Table 5:

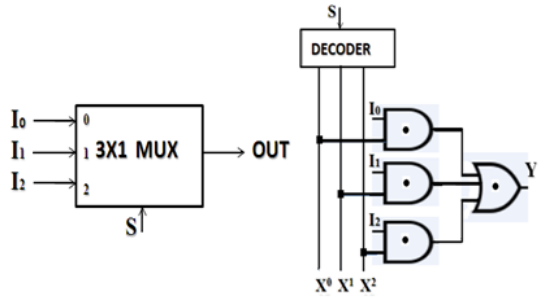


Fig.1.9: Block diagram and circuit diagram of 3x1 MUX

Table 5: Operation Table Of 3x1 MUX

S	OUT
0	I0
1	I1
2	I2

1.5 Design of 9x1 MUX Using 3x1 MUX

A 9x1 MUX is built using four 3x1 MUX as shown in Fig.1.10 and functions as given in Table 6. A 9x1 MUXselects one among the 9 inputs based on 2 select lines.

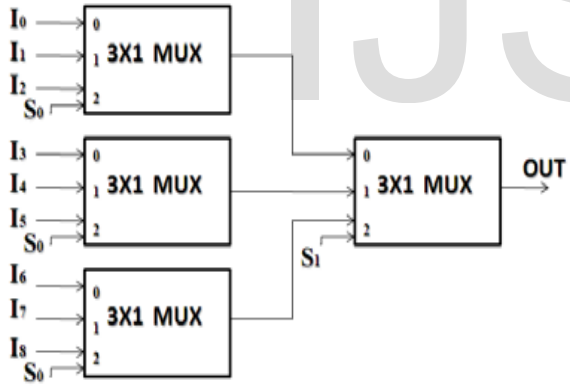


Fig.1.10: Block diagram of 9x1 MUX

Table 6: Function Table Of 9x1 MUX

S1	S0	OUT
0	0	I0
0	1	I1
0	2	I2
1	0	I3
1	1	I4
1	2	I5
2	0	I6
2	1	I7
2	2	I8

3. DESIGN OF HALF ADDER

Ternary half adder is a circuit for the addition two 1 trit numbers is referred to as a half adder. Circuit does not consider a carry generated in the previous addition. Table 7 expresses the addition process in ternary logic system. Here A and B are two inputs and sum(S) and carry (C)are two outputs. Since no grouping of 2's and 1'is possible, the output equation is as here:

Table 7: Truth table for half adder

INPUT		OUTPUT	
A	B	SUM	CARRY
		S	C
0	0	0	0
0	1	1	0
0	2	2	0
1	0	1	0
1	1	2	0
1	2	0	1
2	0	2	0
2	1	0	1
2	2	1	1

B \ A	0	1	2
0		1	2
1	1	2	
2	2		1

B \ A	0	1	2
0			
1			1
2			1

Figure 1.11: Map for half adder SUM and CARRY

Equation for Sum and Carry can be found from the map as follows:

SUM = A2B0 + A1B1A0B2 +1• (A1B0 + A0B1 + A2B2)= 0 +1• (A2B1 + A1B2 + A2B2)

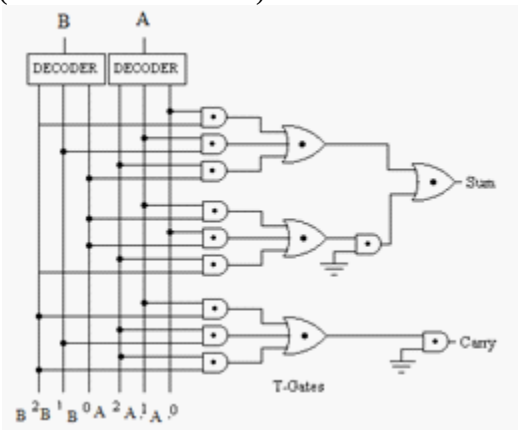


Fig 1.12: Half adder implementation using t-gates

4. FULL ADDER DESIGN

A ternary full adder is a circuit that adds two inputs and previous carry generated. Truth table for full adder is given in Table 5.3 along with K-map in Figure 5.5, 5.6 shows full adder implementation

Table 8: Truth table for full adder

INPUT			OUTPUT	
A	B	C	SUM S	CARRY C
0	0	0	0	0
0	0	1	1	0
0	0	2	2	0
0	1	0	1	0
0	1	1	2	0
0	1	2	0	1
0	2	0	2	0
0	2	1	0	1
0	2	2	1	1
1	0	0	1	0
1	0	1	2	0
1	0	2	0	1
1	1	0	2	0
1	1	1	0	1
1	1	2	1	1
1	2	0	0	1
1	2	1	1	1
1	2	2	2	1
2	0	0	2	0
2	0	1	0	1
2	0	2	1	1
2	1	0	0	1
2	1	1	1	1
2	1	2	2	1
2	2	0	1	1
2	2	1	2	1
2	2	2	2	2

A / B	0	1	2	0	1	2	0	1	2
0		1	2	1	2		2		1
1	1	2		2		1		1	2
2	2		1		1	2	1	2	

Figure 1.13(a) Map for full adder SUM

A / B	0	1	2	0	1	2	0	1	2
0						1		1	1
1					1	1	1	1	1
2		1	1	1	1	1	1	1	2

C=0 C=1 C=2

Figure 1.13(b) Map for full adder CARRY with grouping

K-map equations for sum and carry are as follows:

SUM = A2B0C0 +A1B0C 1+A0B0C2+ A1B1C0+ A0B1C1+A2B1C2 +A0B2C0 +A2B2C1+ A1B2C2 +1 (A1B0C0+A0B0C1+A2B0C2+A0B1C0+A2B1C1+ A1B1C2+A2B2C0+A1B2C1+ A0B2C2)

CARRY =A2B2C2 +1 (A2C2 +A0B2+A2B2 +A1C2 +A2C1 +B2C1 +B1C2 +B2C2 +A1B1C1)

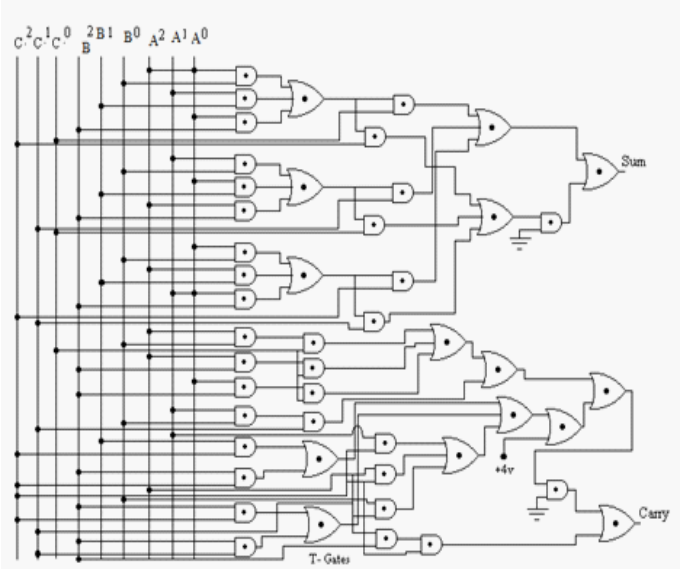


Figure 1.14: Full adder implementation using T-gates

The grounding terminal of sun and carry shows logical grounding of logical 1 for balance System. Decoder block is ternary to unary decoder.

5.CONCLUSION

The ternary logic is a promising alternative to the conventional binary logic design technique. The ternary and binary logic gates can be used to take advantage of their respective merits, to improve performance in terms of computation speed and power consumption. Expanding the existing logic levels to higher levels higher processing rates could be achieved. In this paper, we have defined, analyzed and implemented ternary gates to reduce the gate count in combinational circuits. We have implemented half adder and full adder circuit using ternary gate, here k-map is used for implementation of ternary half adder and full adder.

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